an embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom; and

an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom and connected to the embedded processor via an internal bus;

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a first shared operand unit coupled to the first MAC unit and the second MAC unit for simultaneously providing a first shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other; and

wherein the array processor further comprises:

a second shared operand unit coupled to a third MAC unit and a fourth MAC unit for providing a second shared operand to the third MAC unit and the fourth MAC unit.

10. (Amended) An integrated circuit using a memory, said integrated circuit comprising:

an interface circuit configured to control access to said memory, said interface circuit coupled to said memory;

an embedded processor configured to control said integrated circuit, said embedded processor receiving information from said interface circuit; and

an array processor for performing mathematical calculations on data received from said interface circuit and connected to said embedded processor via an internal bus, said array processor comprising:

a plurality of multiplier/accumulator circuits; and

a plurality of shared operand circuits coupled to said plurality of multiplier/accumulator circuits for simultaneously providing a shared operand to at least two of said plurality of multiplier/accumulator circuits.

23 ~~21.~~ (New) An integrated circuit comprising:

a first embedded processor;

a first array processor coupled to the first embedded processor;

a first memory interface circuit coupled to the first embedded processor and the first array processor;

a first communication port coupled to the first embedded processor;

a second communication port configured to communicate with the first communication port;

a second embedded processor coupled to the second communication port;

a second array processor coupled to the second embedded processor; and

a second memory interface circuit coupled to the second embedded processor and the second array processor.

24 ~~22.~~ (New) The integrated circuit of claim 23 ~~21~~ wherein the array processor comprises:

a first MAC unit coupled a first local memory; and

a second MAC unit coupled to a second local memory.

25 ~~23.~~ (New) An integrated circuit comprising:

a first embedded processor;

an array processor coupled to the first embedded processor;

a memory interface circuit coupled to the first embedded processor and the array processor;

a first communication port coupled to the first embedded processor,

wherein the array processor comprises:

a first MAC unit coupled to a first local memory;

a second MAC unit coupled to a second local memory; and

a shared operand unit coupled to the first MAC unit and the second MAC unit, the shared operand unit for simultaneously providing a shared operand to the first MAC unit and the second MAC unit.

26 ~~24.~~ (New) The integrated circuit of claim ~~23~~ 25 wherein the first communication port communicates with a second communication port, the second communication port coupled to a second embedded processor.